

Electronic Acknowledgement Receipt

EFS ID:	2847487
Application Number:	10787488
International Application Number:	
Confirmation Number:	4982
Title of Invention:	INTEGRATED CIRCUIT LOGIC WITH SELF COMPENSATING BLOCK DELAYS
First Named Inventor/Applicant Name:	Puneet Gupta
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Attorney Docket Number:	YOR920040091US1
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part/.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed	US_IDS_Form__SB_08a.pdf	779966 7118deee882e9590727c7b46cc95081a4 132407487	no	4

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2	NPL Documents	YOR920040091-1.pdf	477200 0d561d6d3de93e85144f77b2fe36c8d 24ee3b29	no	8
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3	NPL Documents	YOR920040091-2.pdf	873807 e9a000d45151394dd0258b7b6eb7a80 8e0ff44ad	no	14
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4	NPL Documents	YOR920040091-3.pdf	810731 8debe65dcab4e4fb1f2a2d9e81535c2 32ed5071	no	13
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5	NPL Documents	YOR920040091-4.pdf	193308 03261a87238e4b9741a3d0246b72865 e5998062	no	9
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